OpenPET Electronics Specification

Revision History

Date	Description
May 1, 2009	Initial Version

http://openpet.lbl.gov

OpenPET was developed as a collaboration between LBNL and SensL

1. System Overview

This document describes the OpenPET electronics architecture. The purpose of the OpenPET electronics is to provide a system that can be used by a large variety of users, primarily people who are developing prototype nuclear medical imaging systems. The system includes hardware, firmware, and software, is scalable enough to provide solutions ranging from a "test bench" for a small number of detector modules to a complete camera, and is "open source" to both maximize flexibility and minimize redundant development.

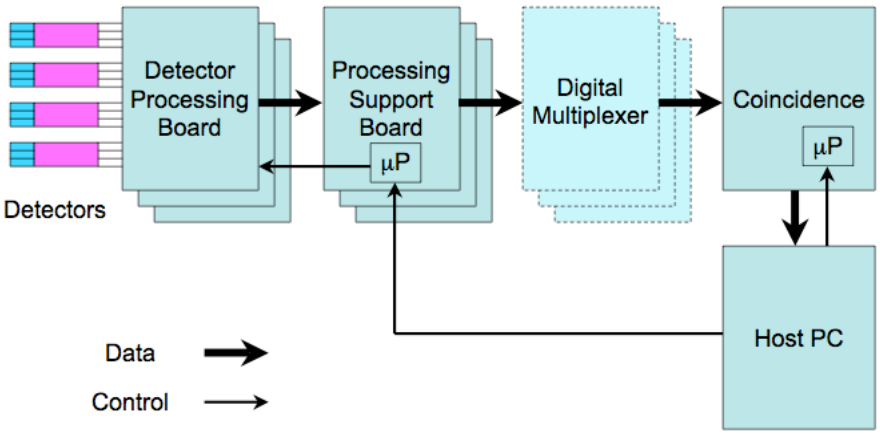

Figure 1

The system architecture is shown in Figure 1. There are four types of custom electronics board in the system: the Detector Processing Board (DPB), the Processing Support Board (PSB), the Digital Multiplexer Board (DMB), and the Coincidence Board (CB). The general data flow is that analog signals from detector modules provide the inputs to the Detector Processing Board. This board processes the analog signals to create a Singles Event Word, which is a digital representation of this single gamma ray interaction. These Singles Event Words are passed to the Processing Support Board, whose main function is to multiplex the Singles Event Words from multiple Detector Processing Boards. The Digital Multiplexer Board is optional - it can provide a further layer of multiplexing for Singles Event Words, if desired. The Coincidence Board searches through the Singles Event Words for pairs that are in time coincidence, and forms a Coincidence Event Word when it does so. These Coincidence Event Words are then passed to the Host PC. Optionally, the Coincidence Board can act as a multiplexer and pass unaltered Singles Event Words to the Host PC. Control Signals originate from the Host PC, are passed to microprocessors that are on the Coincidence Board and Processing Support Board, and are forwarded from there.

The maximum number of each type of board in the system and data rates is described in **Numbers**.

1.1. Numbers

There is a maximum of one Coincidence Board in the system, and there is only one data path from the Coincidence Board to the Host PC. For the time being, we will ignore the optional Digital Multiplexer Board and state that the Coincidence Board can accept inputs from a maximum of eight Processing Support Boards, each of which services one octant of the camera. Coincidences can be formed between any two Processing Support Boards, but coincident pairs that occur within the same Processing Support Board are ignored.

Each Processing Support Board services a maximum of eight Detector Processing Boards, and each Detector Processing Board services a maximum of sixteen analog inputs (note that a conventional PET block detector has four analog outputs, one for each photomultiplier tube). Thus, the system just described can support a maximum

of 1024 analog inputs (16 analog channels per Detector Processing Board, 8 Detector Processing Boards per Processing Support Board, and 8 Processing Support Boards per Coincidence Board), which would correspond to 256 block detector modules.

While this is sufficient for many systems, some designs require many more analog inputs, and the Digital Multiplexer Board can be incorporated into the system between the Processing Support Board and the Coincidence Board to accommodate this. The Digital Multiplexer Board accepts inputs from up to eight Processing Support Boards, multiplexes them, and provides the Coincidence Board with its single output, which is identical to that from a single Processing Support Board. One layer of Digital Multiplexer Boards (eight per system) increases the maximum number of Detector Processing Boards and Processing Support Boards by a factor eight, allowing up to 8192 analog inputs. Each additional layer of Digital Multiplexer Boards increases the maximum number of inputs by another factor of eight. Event rate and dead time must be considered when multiplexing, but is unlikely to be a significant problem. Designs with a larger number of analog channels generally have each channel cover a correspondingly smaller amount of solid angle, making the total event rate for each octant of the camera roughly independent of the number of analog channels.

Although the timing details are described in Timing & Timing Signals, the system divides time into small, fixed length time slices (100-200 ns). All individual operations must occur within a single Time Slice, which implies that only Single Event Words that occur in the same Time Slice can be combined to form a coincident event. While it can take significantly longer than a single Time Slice to fully process a single event, the system is pipelined so that the processing is divided into smaller steps that each can be completed in a single Time Slice. During one Time Slice, each of boards that outputs Singles Event Words (namely the Detector Processing Boards, Processing Support Boards, and Digital Multiplexer Boards) can pass four Singles Event Words. Thus, the maximum singles rate seen at the input of the Coincidence Board is 32 Singles Event Words (four for each of the eight Processing Support Boards) per Time Slice, or approximately 320 million Singles Event Words per second. Similarly, the Coincidence Processor can theoretically identify 448 Coincident Events per Time Slice (16 for each of the 28 Processing Support Board - Processing Support Board combinations), which corresponds to 4.48 billion Coincidence Event Words per second. In practice, the maximum event rate is limited by the transfer rate between the Coincidence Board and the Host PC, which is considerably slower.

1.2. Timing & Timing Signals

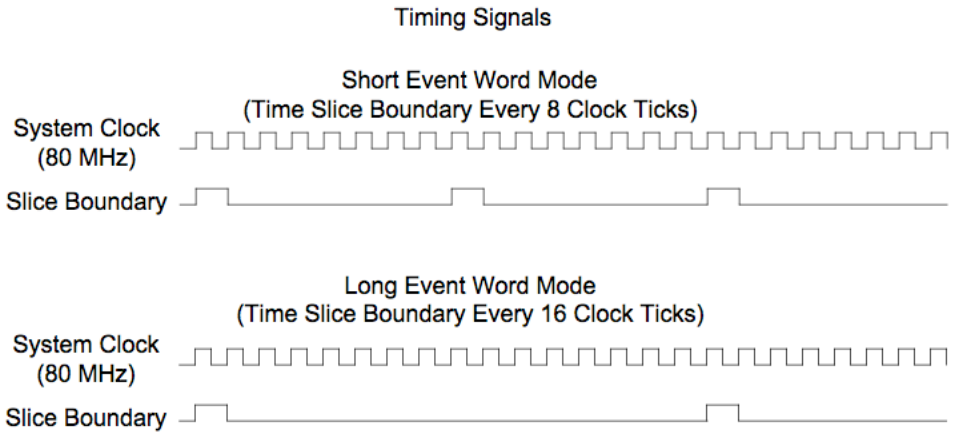

Figure 2

The system level timing signals are shown in Figure 2. There are two timing signals - the System Clock, which is an 80 MHz clock signal, and the Time Slice Boundary, which defines the beginning of a Time Slice. The firmware will support both “short” and “long” event words. In “short” mode, the Time Slice Boundary is generated every eight System Clock cycles, while in “long” mode it is generated every sixteen System Clock cycles. The choice

creates a tradeoff – in “short” mode the dead time is a factor of two shorter but the number bits per event word is also a factor of two smaller.

1.2.1. System Clock

The System Clock is 80 MHz clock. It is generated on the Coincidence Board, then buffered through the rest of the system. Propagation delays will introduce skewing, therefore each FPGA that outputs data will also output a copy of the System Clock that is synchronized with its output data signals.

1.2.2 Time Slice Boundary

The rising edge of the Time Slice Boundary defines the beginning of a Time Slice. The width of the pulse is one System Clock cycle, and the period is eight System Clock cycles (for “short” event word mode) or sixteen System Clock cycles (for “long” event word mode). It is generated on the Coincidence Board, and then buffered through the rest of the system. Propagation delays will introduce skewing; therefore each FPGA that outputs data will also output a copy of the Time Slice Boundary that is synchronized with its output data signals.

1.2.3 Time Slice

The system divides time into small, fixed length Time Slices (100-200 ns). All individual data processing operations must occur within a single Time Slice, which implies that only Single Event Words that occur in the same Time Slice can be combined to form a coincident event. While it can take significantly longer than one Time Slice to fully process a single event, the system is pipelined so that the processing is divided into smaller operations that each can be completed in a single Time Slice. It takes one Time Slice to transfer either a Singles Event Word or a Coincidence Event Word.

2. Detector Processing Board

The purpose of the Detector Processing Board is to accept analog inputs from the detectors and convert them into Singles Event Words. Generally speaking, this requires identifying the energy, interaction position, and arrival time associated with a single gamma ray interaction, and as many corrections as possible should be applied before the Singles Event Word is generated. This board must also have the ability to produce "singles events" that have Alternate Event Formats, which are necessary for debugging, calibration, etc.

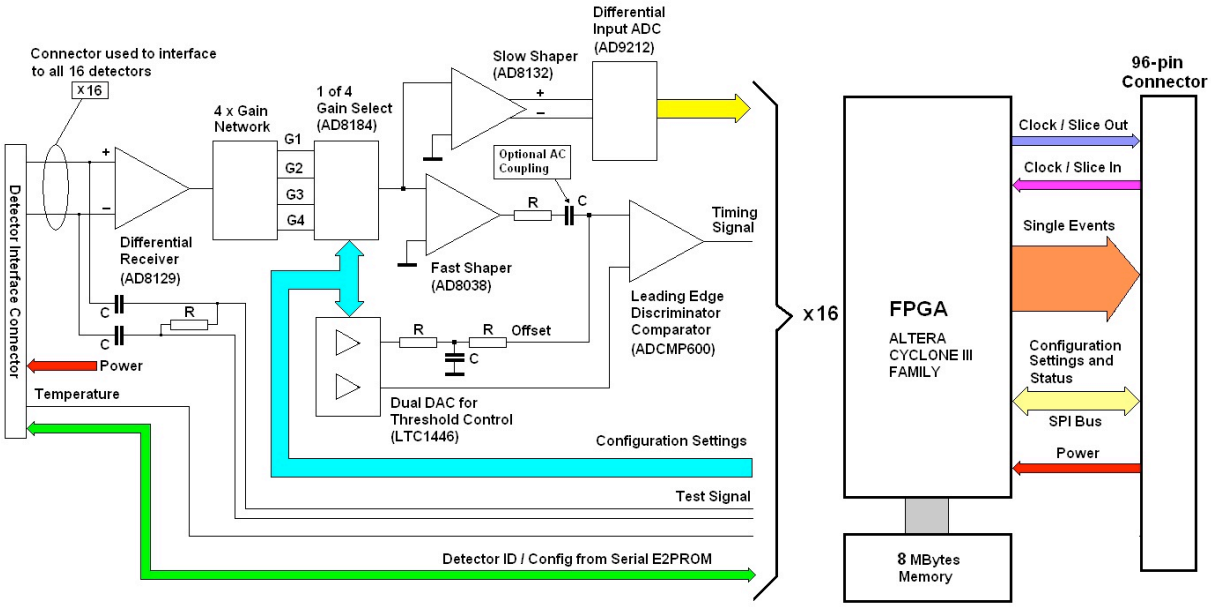

Figure 3

The Detector Processing Board, which is shown schematically in Figure 3, accepts up to 16 analog input signals, each of which is processed independently. The processing circuit for one channel consists of a variable gain amplifier that converts the input signal to the proper polarity, provides gain to match it to the ADC range, and does low-pass anti-alias filtering. The filtered signal is sent to an ADC that digitizes the analog signal every System Clock cycle. A full-bandwidth version of the amplified signal is also created, and is sent to a Timing Signal circuit. This is a discriminator that converts the analog signal into a digital timing signal whose leading edge is synchronized to the interaction time. The ADC values and the Timing Signal are sent to the Detector FPGA.

Inside the Detector FPGA, a TDC generates a time stamp indicating the arrival time of the Timing Signal relative to the Time Slice Boundary. The Detector FPGA and its Detector Memory also analyzes the ADC data from this channel and (potentially) combines it with information from other channels to compute the energy deposit, the interaction position, and the event time. Appropriate calibration correction factors are also stored in the Detector Memory and applied to the data. The Detector FPGA also generates Test Pulse signals that can be injected into the analog inputs for testing and debugging, as well as provides the Bus IO.

2.1 Analog Conditioning

Figure 3 includes a schematic of the Analog Conditioning circuit. Each circuit has an input a analog signal, which can either be directly from a detector or the output of an earlier stage of preamplification / amplification. Each

input signal is passed through an amplifier that converts it into the proper polarity for the ADC, has adjustable gain in order to match the input range of the ADC, and an appropriate low pass filter to eliminate aliasing. Another amplifier drives the Timing Signal circuit and provides appropriate gain. As the highest timing accuracy is obtained with high bandwidth signals, this amplifier does not include a low pass filter and has a bandwidth of ~200 MHz.

The input stage accepts voltages between –2V and +2V and has input diodes to protect against over voltage. A single resistor terminates the input, typically with either 50 or 100 Ohms. As the input is differential, detector signals of either polarity can be accommodated by selecting which inputs (positive or negative) to connect them to. Optionally, one can ground either of the inputs, allowing single-ended signals of either polarity to be accepted. Any of four gains, spanning a 5:1 range, can be selected via computer control.

2.3 Timing Signal

This circuit is a high-speed leading edge discriminator with a threshold that is controlled via a DAC. The timing edge is a low to high transition.

2.3 ADC

Each analog input signal is digitized by a 10-bit ADC that converts (and is read out by the Detector FPGA) every System Clock cycle (80 MHz).

2.4 Detector FPGA

A significant amount of computation is necessary in order to convert the detector signals into a Singles Event Word. This is done by the Detector FPGA and its associated Detector Memory. Programs are loaded into the Detector FPGA by the Processing Support Board as described in the Bus IO Section.

While the details of the signal processing depend strongly on the details of the detector module, the following is an example describing the processing performed for a block detector module with four analog outputs. Event processing is initiated by the OR of the low to high transitions from each of the Timing Signal. The total amount of signal observed by each of the four PMTs (A, B, C, & D) is computed by summing the output of each ADC for an appropriate period of time (typically 2-3 times the decay time of the scintillator). If necessary, pulse pile-up correction is also applied. These four signals are then summed to get a raw estimate of the energy (E=A+B+C+D), and the appropriate Anger logic estimators are computed (X=(A+B)/E, Y=(A+C)/E). Note that a fast division algorithm can be implemented using look-up tables in the Detector Memory. The X and Y values are used to address a crystal map table that resides in the Detector Memory, and so assign a crystal of interaction via a look-up table. The raw energy E and the crystal of interaction are again used to address another look-up table in the Detector Memory, and so determine whether the event satisfies the energy window criteria. Each Timing Signal is input to a TDC that is implemented in the Detector FPGA, and so measures the (raw) position of the arrival time of each signal within a Time Slice, and a timing estimator computed from these digitized arrival times. The crystal of interaction and raw arrival time are used to address a look-up table stored in Detector Memory and create a corrected arrival time. Thus, the position (crystal of interaction), energy, and arrival time have all been computed. If the event satisfies the energy window criteria, these data are formatted to create a Singles Event Word, and then passed to Processing Support Board through the Bus IO block.

Note that different programs can be loaded into the Detector FPGA to perform tasks other than event processing, such as several types of debugging, testing, and calibration tasks.

2.5 TDC

The TDC digitizes the arrival time of the Timing Signal with respect to the Time Slice Boundary. Thus, its minimum and maximum counts correspond to the beginning and end of a single Time Slice respectively. The TDC is synchronized to the System Clock, which is used to create the higher order bits of the TDC. However, the granularity of the System Clock is too coarse for PET, and so the TDC must generate a minimum of four additional low order bits of timing data. Thus, the least bit of the TDC will be 0.8 ns or smaller.

2.6 Detector Memory

8 MBytes of SRAM memory is attached to and controlled by the Detector FPGA. This control also includes loading the contents of the memory.

2.7 Test Pulse

The Detector FPGA creates separately controlled digital signals that are attenuated and fed into each analog input of the board. These signals, which mimic real analog input signals, are used for testing and calibration.

2.8 Bus IO

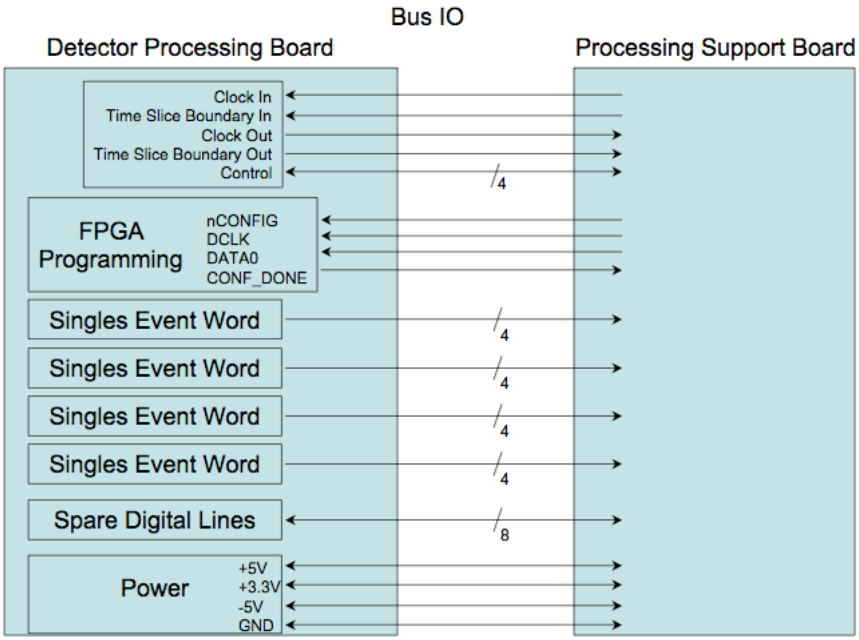

Figure 4

A diagram of the Bus IO is shown in Figure 4. One block essentially provides control signals. A copy of the System Clock and Time Slice Boundary signals are sent from the Processing Support Board and are used to clock data from the Processing Support Board to the Detector Processing Board. Because there is propagation delay within the Detector Processing Board, another copy of the System Clock and Time Slice Boundary that is produced by the Detector Processing Board is used to clock data from the Detector Processing Board to the Processing Support Board. Eight additional “spare” lines can be used to pass bi-directional information between

boards. Lines controlled by the Processing Support Board are used to program the Detector FPGA on the Detector Processing Board. Finally, there are lines that can simultaneously pass four Singles Event Words from the Detector Processing Board to the Processing Support Board in a combination serial / parallel protocol. For each Singles Event Word, one bit of data is passed on each of four parallel lines during each System Clock cycle, with the entire Singles Event Word being passed during a single Time Slice.

2.9 Connections to Processing Support Board

Pin Assignment for the Connector Between the DPB and the PSB

	A	B	C
1	D0+	GND	D1+
2	D0-	3.3V	D1-
3	D2+	GND	D3+
4	D2-	+5V	D3-
5	D4+	GND	D5+
6	D4-	-5V	D5-
7	D6+	GND	D7+
8	D6-	3.3V	D7-
9	D8+	GND	D9+
10	D8-	+5V	D9-
11	D10+	GND	D11+
12	D10-	-5V	D11-
13	D12+	GND	D13+
14	D12-	3.3V	D13-
15	D14+	GND	D15+
16	D14-	+5V	D15-
17	GND	-5V	GND
18	CLK_IN+	3.3V	CLK_OUT+
19	CLK_IN-	+5V	CLK_OUT-
20	GND	-5V	GND
21	SLICE_IN+	3.3V	SLICE_OUT+
22	SLICE_IN-	GND	SLICE_OUT-
23	GND	NC	GND
24	SPARE0+	SPARE1+	SPARE2+
25	SPARE0-	SPARE1-	SPARE2-
26	SPARE3+	SPARE4+	SPARE5+
27	SPARE3-	SPARE4-	SPARE5-
28	SPARE6+	SPARE7+	CTRL_CS
29	SPARE6-	SPARE7-	CTRL_CLK
30	CTRL_DO	NC	CTRL_DI
31	DCLK	DETECTOR BIAS	DATA0
32	nCONFIG	3.3V	CONF_DONE

Color	Group Description
	LVDS Data to DPB FPGA & Coincidence Board
	Clock & Slice IN/OUT
	Undefined pins between DPB FPGA & DSB FPGA
	Slow control SPI interface signals
	DPB FPGA serial programming pins
	No connection
	Power & GND
	Detector Bias Voltage (100 V max.)

Connector is
96 pin VME Connector
(DIN41612 Type C)

Figure 5

Figure 5 and the following section detail the connections between the Processing Support Board and the Detector Processing Board.

Singles Event Data

There will be 16 LVDS differential pairs that are used to transfer digital Singles Event Words from the Detector Processing Board (DPB) to the Processing Support Board (PSB).

Clock

There will be 4 LVDS differential pairs that are used to transfer digital timing signals between the Detector Processing Board (DPB) and the Processing Support Board (PSB). A Clock In and Time Slice Boundary In will be sent from the PSB to the DPB, and data going from the PSB to the DPB will be synchronous with these clock signals. Similarly Clock Out and Time Slice Boundary Out will be sent from the DPB to the PSB, and data going from the DPB to the PSB will be synchronous with these clock signals.

Control

There will be 4 LVTTL single ended lines used to pass control data from the PSB to the DPB. They will use a variant of the SPI (Serial Peripheral Interface) Bus protocol, which consists of a Clock line, a Data In line, a Data Out line and a Board Enable line.

FPGA Programming

There will be 4 single ended LVTTL lines used to program the FPGA using the serial protocol. These signals will be provided by the PSB.

Spare Digital

There will be 8 LVDS differential pairs between the FPGAs on the PSB and the DPB. Their purpose is presently undefined, but the intent is to provide users flexibility in passing information between the two boards. However, they are likely to come in handy if we need to make revisions.

Power and Ground

The PSB will supply power to the DPB. It will supply +5V, +3.3V, -5V, ground, and a detector bias voltage (100V maximum). With the exception of the detector bias voltage, it is assumed that this is “digital quality” power – that the DPB will use these as inputs to on-board regulators to create analog quality power, as well as whatever other digital voltages are necessary. It is also assumed that the +3.3V will be used to supply power for the digital components, while the +5V and -5V will be used to supply power to the analog components.

Connector

We will use the same 96-pin connector as is used in VME modules, which is a DIN 41612 Type C. Note that the pin assignment is not compatible with the VME standard, and so the OpenPET electronics CANNOT be plugged into VME crates.

3. Processing Support Board

The main purpose of the Processing Support Board is to accept Singles Event Words from multiple Detector Processing Boards, multiplex them, and pass these Singles Event Words to the Coincidence Board. In addition, it provides the control and power for the Detector Processing Boards, and is the interface with the Host PC. It can also be configured to act as low-performance version of a Coincidence Board, and so identify coincident events and pass them to the Host PC.

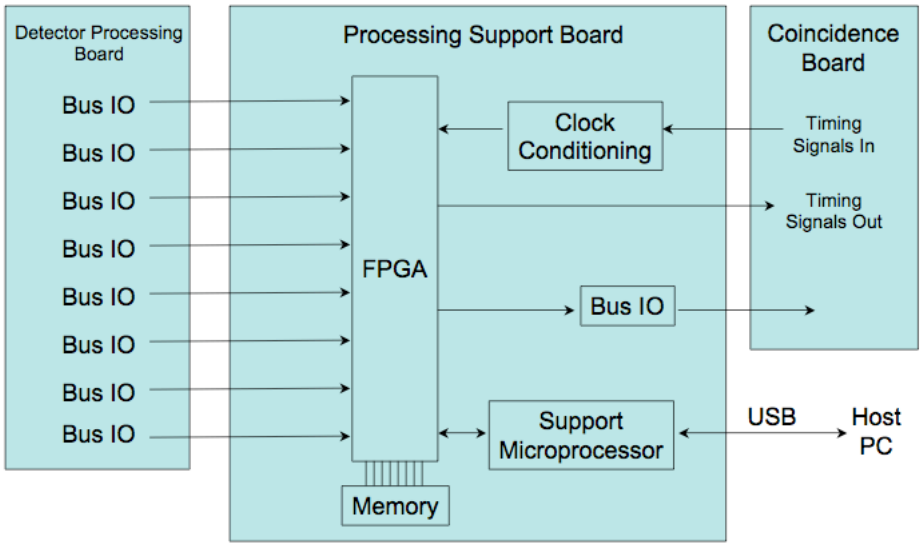

Figure 6

The Processing Support Board, shown schematically in Figure 6, services up to 8 Detector Processing Boards. A separate Bus IO circuit connects the Support FPGA to each Detector Processing Board. The Support FPGA (possibly with the help of Support Memory) multiplexes the Singles Event Words and passes them through a ninth Bus IO block to the Coincidence Board. A Clock Conditioning block ensures the fidelity of the System Clock.

High-level commands are sent via USB to a Support Microprocessor from the Host PC, which interprets and executes these commands. This execution may involve controlling the Detector Processing Board, such as by loading a program into the Detector FPGA on the Detector Processing Board, or may involve higher level functions, such as performing a calibration by instructing the Detector Processing Board to produce calibration data, analyzing the forthcoming calibration events, computing calibration parameters, and loading these parameters into the Detector Memory on the Detector Processing Board. The Support Microprocessor also loads the program into the Support FPGA.

The Support FPGA is also capable of identifying coincident pairs of Singles Event Words, format them into Coincidence Event Format, and pass them to the Support Microprocessor, which then passes them to the Host PC. Thus it can act as a full-featured PET data acquisition system, albeit with a limited number of input channels and output event rate capability.

3.1 Support Microprocessor

The Support Microprocessor is connected via USB to the Host PC, from which it receives high-level commands, and then interprets and executes these commands. It is responsible for storing and loading all the programs in

both the Support FPGA and Detector FPGA, the contents of all the Support Memory and Detector Memory, and all of the other registers that are on the Detector Processing Board and Processing Support Board. It monitors the event stream and can insert diagnostic information (such as event rates) into the event stream or provide this information directly to the Host PC. Whenever possible, calibration routines are also performed on the Support Microprocessor.

3.2 Support FPGA

The Support FPGA primarily acts as a multiplexer for Singles Events, taking the up to 32 individual Singles Events that it can receive in a single Time Frame and passing up to 4 of them to the Coincidence Processor. Obviously, there is some possibility for data loss, and the multiplexing algorithm is designed to ensure that this loss is unbiased. The Support FPGA also serves as a fan-in / fan-out for communication between the Support Microprocessor and the individual Detector Processing Boards.

3.3 Support Memory

8 MBytes of SRAM memory is attached to and controlled by the Support FPGA. This control also includes loading the contents of the memory.

3.4 Clock Conditioning

The Clock Conditioning block consists of a PLL (phase-locked loop) that regenerates the System Clock signal from the Coincidence Board and passes it to the Support FPGA and then to the Detector Processing Boards. The block also includes space for a clock IC, which is used to provide the System Clock when the system is being used without a Coincidence Board (i.e. when the Support Microprocessor passes events directly to the Host PC).